Abstract—This paper deals with the implementation of a PC-controlled benchmark specially suited to real-time experimental investigation of oscillators driven by impulsive parametric pulses. The benchmark performs both the acquisition of the output signal and the generation of the parametric pulses. It also allows the introduction of a programmable delay to investigate its influence on the dynamics of the oscillator. The time required for the building of each pulse has been reduced from 10 ms (typical setting time of a standard programmable generator) to 15 μs, employing the standard PC’s direct memory access (DMA) transfer and pulse generation capabilities, allowing the investigation of oscillators with relevant frequency content up to 30 kHz.

Index Terms—A/D conversion, chaos, data acquisition, direct memory access (DMA) transfer, nonlinear oscillators, phase portraits, synchronization.

I. INTRODUCTION

Nonlinear oscillators driven by periodic forces appear in many problems in physics and other sciences [1]-[10]. In the very common case of impulsively driven oscillators, the external perturbation consists of very short pulses (to be referred hereafter as “kicks” [11]-[14]). An interesting behavior arises in systems with a parametric feedback [13]-[14]. A typical parametrically kicked oscillator works as follows. The oscillator has a free running period \(T_o\). It is excited by a driving signal which is a pulse train with period \(T_E\), width \(\Delta E\), and amplitude \(A_E\). The output signal is sampled every \(T_E\) s and after each sample a kick is sent, its amplitude \(A_E\) being a function of the measured value. There always exists a delay \(\tau\) between the sampling time and the kicking time, most commonly in the way of the finite time required for performing the measurement of the control variable and acting accordingly. This delay has been reported as a major obstacle to the successful control of some oscillatory chemical processes [15]. On the opposite side, a method has recently been proposed for controlling chaos by using this very same delay [16]-[20].

In this kind of experiment, a large amount of data must be stored and analyzed in order to capture the relevant dynamics, especially if chaotic behavior is to be expected. The central objective of this paper is the implementation of an efficient benchmark, capable of producing a real-time simulation of this kind of system. The benchmark uses the power and flexibility of PC’s to control standard instrumentation and requires only a minimum of additional low-cost circuitry. The proposed benchmark is shown schematically in Fig. 1. Block 1 is the dynamical system under investigation. It may be any kind of oscillator, not only an electronic one, but suited transducers should be included. It has an input (IN) where the kicks are applied and an output (OUT) which is the signal of interest. Block 2 is a generator capable of producing a periodic train of pulses with programmable frequency. It works as a master generator for the measurement arrangement. Block 3 is the heart of the benchmark: the multifunction data acquisition board (MFDAB) developed in our laboratory; it performs both the oscillator’s output sampling and digitizing process, and the generation of the delayed kicks. It also includes the IEEE-488 interface for controlling the master generator mentioned above.

Fig. 2 depicts the overall timing diagram. In Fig. 2, the curve labeled (a) is a typical output signal under study (measurement point 1 in Fig. 1); (b) is the output of the master generator (measurement point 2 in Fig. 1); and (c) is the sampled signal, samples being taken at a rate \(1/\Delta t\). The samples labeled \(X_1, X_2, X_3, \ldots\) are those employed to construct the parametric kicks. (d) is the periodic stimulus, each one being proportional to the value of the signal at \((t - \tau)\) (\(\tau\) is the delay). In Fig. 2, \(T_B\) is the “building time” required to build the next kick (see below).

During an actual simulation, both the period \(T_E\) and the width \(\Delta E\) of the kicking signal are chosen at the beginning of the measuring process as they remain constant afterwards. On
Fig. 2. Overall timing chart for the case of a typical oscillator.

the other hand, the amplitude $A_E$ of the kicks is an arbitrary function of the oscillator signal output selected by the user. This amplitude is allowed to vary from pulse to pulse. In our benchmark, we have expressly set all programmable times as multiples of $\Delta t$.

Time $t_B$ is the critical variable that limits the maximum frequency attainable in the process. There are several reasons for this. First, during the building time $t_B$ the machine is unable to acquire any sample at all and so in order to avoid losing samples, one has to choose $\Delta t$ greater than $t_B$. Second, the Nyquist criterion for sampling states that $f_{\text{max}}$ must be lower than $1/(2t_B)$ in this case. $f_{\text{max}}$, the maximum relevant frequency in the Fourier spectrum of the output signal. Third, the delay $\tau$ must be a fortiori (i.e., by physical constraints) greater than $t_B$.

For low-frequency oscillators, parametric kicks can be built by means of a standard programmable function generator controlled via an IEEE-488 interface. This procedure implies a building time of about of 10 ms (the typical setting time of a programmable generator) and then only oscillators with relevant frequency content up to 50 Hz can be investigated. In this paper, we show how the capabilities of standard PC's can be exploited in order to reduce this time $t_B$ to 15 $\mu$s. Our acquisition board is connected to the ISA-BUS and then the value of $t_B$ is limited by the characteristics of the BUS and is independent of the PC employed. In fact, we have checked this value with a 386 PC, a 486 DX2 66 MHz PC, and a 486 DX4 100 MHz PC.

This paper is organized as follows. In Section II a brief description of standard PC's direct memory access (DMA) capabilities is included; Section III deals with the general description of the MFDAB and its DMA manager. In Section IV, both the complete block diagram of the card and the software flow-diagram are detailed. Conclusions are presented in Section V.

II. STANDARD PC'S DMA TRANSFER CAPABILITIES

DMA provides a method for high-speed transfer of data between memory and the I/O bus, where the peripherals, and also our MFDAB, are to be connected. To perform this function, PC's based on the 80x86 processors family, have two special integrated circuits (IC's): the 82x37 DMA controllers DMA1 and DMA2, each one containing four separate DMA channels and a number of registers to control the DMA operations, to specify the number of bytes/words to transfer, and to designate the memory addresses for the transfer. These registers are all accessed through I/O ports. DMA1 and DMA2 are both connected to several control lines: eight DRQ (DMA request) and DACK (DMA acknowledge) lines, one for each channel, the HRQ (hold request) line, the HACK (hold acknowledge) line and the TC (terminal count) line. DRQ and DACK lines are all available on the extension bus (ISA) [21]. In this paper, channel 1 and its corresponding registers and control lines are used.

Once the setting-up procedure has been finished, the 82x87 takes under its own control both the data and the address busses and drives the processor into a HOLD state in order to make the data transfer faster than it could be done under the processor supervision. There are several transfer modes available, the single mode being the one used in this work. In this particular mode, the transfer process starts with a peripheral device request. By setting the DRQ line to the programmed request level ("high" in our case) the 82x37 drives the DACK line to "low" to enable the datum to be transferred from the peripheral device into memory. This process repeats for each datum until the end of the block is reached.

Several internal 82x37 registers are used in order to initiate, enable, and monitor all the DMA processes. The processes are: the Base address and base word count, current address and current count registers (one for each channel), and the mask, status, and mode registers (one for each DMA-IC). In Fig. 3, the DMA controller architecture is summarized. The base address register holds the starting address, where data storage starts. It is copied to the current address register during the initialization procedure. After each transfer, this last register is automatically incremented and then it stores continuously the value currently in use. The base word count register stores the total number of data to be transferred. It is copied to the current count register during the initialization procedure. This last register is automatically decremented after each transfer as it contains the number of the remaining transfer cycles to be done. Once this register reaches 0, a terminal count (TC) signal is generated, indicating the completion of the DMA transfer sequence. The 8-bit page register is added as to extend the memory accessed to 16 Mbytes. The mask, mode, and status registers allow the full selection of the DMA transfer process characteristics. A brief description of allowed options, and the particular settings employed in this work, is shown in Fig. 4.
III. DATA ACQUISITION AND DMA MANAGER CIRCUITS

Data acquisition boards are used extensively in several fields of science and engineering. The exact triggering of the A/D converter is a critical issue because a slight variation in the period between samples could lead to fatal distortions in the data stream, especially when delicate measurements are involved [22]. Conversion must be started under the control of the acquisition board’s own clock in order to assure the total independence of the sampling process from the PC’s special features.

The block diagram of the MFDAB developed here is shown in Fig. 5. It works as follows. The connector C has nine pins; eight of them are inputs to the input mux 8-channel block while the ninth receives the pulses from the function and pulse generator block. Pin 1 is shared with the trigger circuitry, and the master generator output signal is connected to this pin for synchronization purposes as explained below. The selected channel (channel 2 in our case) is fed to the programmable gain amplifier block which performs the signal level conditioning. The voltage gain of this block is programmable and full-scale voltages from 50 mV up to 50 V are allowed. The output signal of this programmable gain amplifier is fed into the 12-bit A/D converter block which makes the conversion. The sampling rate is controlled by the timing control circuit block and the digitized samples are transferred to the PC RAM through the DMA circuit controller block.

The acquisition process starts up when the signal of the master generator, which is connected to channel one, reaches the trigger level fixed in the D/A trigger level block. The comparison is made by the trigger circuit block, which generates the gate signal (GS). The initialization of the registers is achieved by the address decoder block.

As DMA single transfer mode allows for a synchronization between sampling and transfer instants, it is especially well-suited for use in this sampling process, its operation being controlled by the timing control block through the synchronism pulse (SP). This procedure has the advantage of requiring no additional memory on the data acquisition board. The DMA circuit controller block is shown in detail in Fig. 6. This circuit generates the DRQ1 signal by taking the synchronism pulse SP and the gate signal GS. Both signals (SP and GS) are sent to the inputs of a NAND gate (IC2A and IC2D) its output being connected to the clock input of the FF-JK IC3A. The output Q of this flip-flop is the DRQ1 signal. This last signal goes up to “high” and it remains in this state until the PC acknowledges the request by pulling down the DACK1 line to “low.” Then the access requirement ends and the output of the FF-IC3A is reset by IC2B through IC2C. This same IC2C output enables the A/D converter IC1.

The input-output read (IOR) signal coming from the PC bus, is connected to the ReaD line (RD) of the 12-Bit A/D converter block allowing the transfer. Since the FF-IC3B clock input is connected to the DACKl line, this FF changes its state each time a datum is transferred to memory. In this way, by means of the high byte enable (HBEN) line, the words 12 bits are sequentially read through the converter data lines (D0 to D7), the eight lower order bits first and then the four remaining higher order bits. The data acquisition and DMA transfer timing charts are shown in Fig. 7.

The MFDAB also includes a pulse generator block. In our case, it is used only as a programmable digital to analog converter and it generates the pulses, once the programmed delay \( \tau \) is reached.

IV. GLOBAL PROCESS AND ADDITIONAL HARDWARE DESCRIPTION

The complete process is described in Fig. 8 (see also the timing diagram of Fig. 2). The process is as follows. 1) The master generator frequency \( (1/T_F) \) is fixed using the IEEE interface included into the MFDAB. 2) The number of periods
$N_p$ and the sampling rate $(1/\Delta t)$ are initialized; $1/\Delta t$ is selected to be equal to $N_t \cdot (1/T_E)$, i.e., an integer multiple of the master generator frequency (minimum $\Delta t$ is 15 $\mu$s). 3) Mode, base address, and base word count registers are set to the values indicated in Fig. 4. The delay is given by $N_1 \cdot \Delta t$ and this $N_1$ value is stored in the base word count register (minimum $N_1$ is 1). 4) The DMA is enabled. 5) Now, the next pulse of the master generator triggers data acquisition in channel two of the MFDAB, where the oscillator output is connected. 6) As soon as the first sample is acquired, the amplitude $A_E$ of the next kick to be applied is calculated. This amplitude may be any function of the sample value. 7) Once $N_1$ samples have been transferred to memory (i.e., when the delay $\tau$ has elapsed) the second lowest bit of the DMA status register goes "high" indicating that a kick must now be applied to the oscillator. 8) The width $\Delta E$ of this kick is fixed by setting a new number $N_2$ into the DMA base word count register, $\Delta E$ being equal to $N_2 \cdot \Delta t$. Steps 6), 7), and 8) require a minimum $t_B$ of 15 $\mu$s (as was explained in Section I). 9) Acquisition continues and when $N_2$ new samples have been acquired, the second lowest bit in DMA status register goes "high" again indicating that the DAC has to be reset because the excitation has finished. 10) The remaining number of samples, i.e., $N_3 = N_t - N_1 - N_2$, is stored in the DMA base word count register and the second lowest bit of the DMA status register is set to "low" enabling data acquisition again.
Fig. 7. Timing chart for the DMA transfer process.

until the total number of samples \( N_3 \) has been acquired. 11) With the next master generator pulse, the process restarts, and steps 5)–10) are repeated with frequency \( 1/T_E \) until the total number of periods \( N_p \) is reached. 12) Data stored in memory are saved to the hard disk for later analysis.

V. CONCLUSIONS

The technique developed here has the following remarkable characteristics. DMA capabilities of a PC have been utilized, and the processing time has been reduced from 10 ms to 15 \( \mu s \) allowing real-time measurements in oscillators with relevant frequency content up to 30 kHz.

ACKNOWLEDGMENT

The authors would like to thank D. R. Avalos for helpful discussions during the preparation of this paper. They also thank F. Tomasel for his collaboration.

REFERENCES


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